Keysight Technologies
Modifying DDR Libraries for Silicon Nail Test Generation on the x1149 Boundary Scan Analyzer
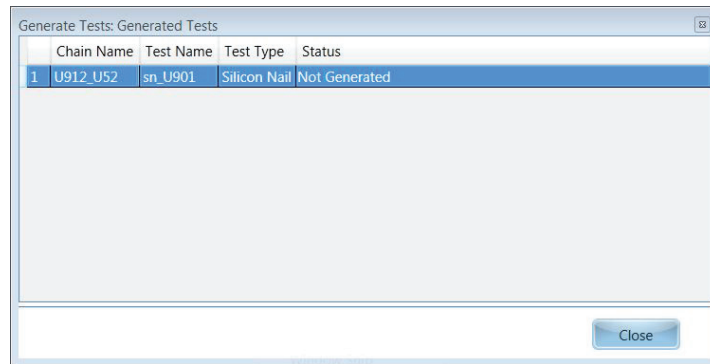
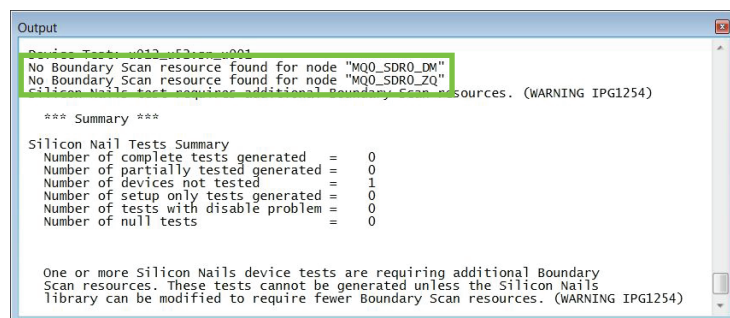Application Note

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The DDR libraries available are written with the assumption that all the pins are connected to a boundary scan cell. In a real board application however, there are pins that are not connected to boundary scan cells, in which case we will need to modify the DDR library to generate the silicon nail test.

Here are the step-by-step procedures on DDR library modification and silicon nail test generation.

1. When silicon nail test is not generated during the Keysight Technologies, Inc. x1149 test:
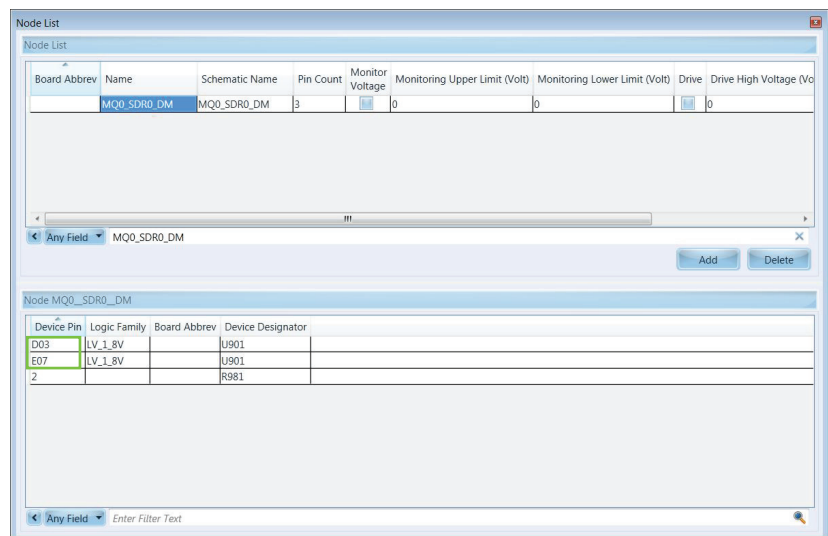
Generate Tests: Generated Tests

	Chain Name	Test Name	Test Type	Status
1	U912_U52	sn_U901	Silicon Nail	Not Generated

Close

2. Check the output message:

Output

```
Device Tests u912 u52 sn u901
No Boundary Scan resource found for node "MQ0_SDR0_DM"
No Boundary Scan resource found for node "MQ0_SDR0_ZQ"
Silicon Nails test requires additional Boundary Scan resources. (WARNING IPG1254)

   *** Summary ***

Silicon Nail Tests Summary
   Number of complete tests generated   =   0
   Number of partially tested generated =   0
   Number of devices not tested         =   1
   Number of setup only tests generated =   0
   Number of tests with disable problem =   0
   Number of null tests                 =   0


   One or more Silicon Nails device tests are requiring additional Boundary
   Scan resources. These tests cannot be generated unless the Silicon Nails
   library can be modified to require fewer Boundary Scan resources. (WARNING IPG1254)
```

The output message shows that the following nodes "MQ0_SDR0_DM" and "MQ0_SDR0_ZQ" are not connected to a boundary scan cell or resource.

3. Check the board details to find out if the "MQ0_SDR0_DM" and "MQ0_SDR0_ZQ" are connected to a DDR and the boundary scan device pins.

Node List

Node List

Board Abbrev	Name	Schematic Name	Pin Count	Monitor Voltage	Monitoring Upper Limit (Volt)	Monitoring Lower Limit (Volt)	Drive	Drive High Voltage (Vo
	MQ0_SDR0_DM	MQ0_SDR0_DM	3		0	0		0

Any Field ▼ MQ0_SDR0_DM

Add   Delete

Node MQ0_SDR0_DM

Device Pin	Logic Family	Board Abbrev	Device Designator
D03	LV_1_8V		U901
E07	LV_1_8V		U901
2			R981

Any Field ▼ Enter Filter Text

4. The node "MQ0_SDR0_DM" in the node list shows the DDR pins D03 and E07 are shorted and connected to resistor "R981" and the pull down is set to "GND".

5. Do the same for the other node "MQ0_SDR0_ZQ", which is connected to resistor "R971", with the pull down set to "GND".

6. The nodes "MQ0_SDR0_DM" and "MQ0_SDR0_ZQ" are not connected to any boundary scan cell or resource. This is the reason why the silicon nail test could not be generated.

7. In order to generate the silicon nail test for the u901 DDR3, the DDR3 library has to be modified as follows:

   7.1 Change the pin usage of the group DM (u901.E07 and u901.D03) and ZQ (U901.L08) from inputs to non-digital.

   7.2 Comment the vector where the DM and ZQ are declared.

```
assign CK        to pins "J07"
assign CK_       to pins "K07"
assign CKE       to pins "K09"
assign CLK       to pins "J07" ,"K07"

assign CS_       to pins "L02"
assign RAS_      to pins "J03"
assign CAS_      to pins "K03"
assign WE_       to pins "L03"
assign COMMAND   to pins "L02","J03","K03","L03"
assign DM        to pins "E07","D03"

assign BA2       to pins "M03"
assign BA1       to pins "N08"
assign BA0       to pins "M02"

assign Address   to pins "N07","R07","L07","R03","T08"
assign Address   to pins "R02","R08","P02","P08","N02","P03","P07","N03"

assign DQ        to pins "A03","B08","A02","A07","C02","C08","C03","D07"
assign DQ        to pins "H07","G02","H08","H03","F08","F02","F07","E03"

assign DQS       to pins "F03","G03","C07","B07"

assign VDD       to pins "B02","D09","G07","K02","K08","N01","N09","R01","R09"
assign VDDq      to pins "A01","A08","C01","C09","D02","E09","F01","H02","H09"
assign Vref      to pins "H01","M08"

assign VSS       to pins "A09","B03","E01","G08","J02","J08"
assign VSS       to pins "M01","M09","P01","P09","T01","T09"
assign VSSq      to pins "B01","B09","D01","D08","E02","E08","F09","G01","G09"

assign ODT       to pins "K01"
assign ZQ        to pins "L08"
assign RES       to pins "T02"
```

```
power VDD,VDDq,VSS,VSSq,Vref

inputs CK,CK_,CKE,CS_,RAS_,CAS_,WE_,BA0,BA1,BA2 !!!DM commented DM not connected to bscan cell
inputs COMMAND
inputs Address
inputs ODT,RES !!! ZQ commented ZQ not connected to bscan cell

bidirectional DQ, DQS

nondigital NC,DM,ZQ
```

```
vector Initialize_inputs
 drive DQ, DQS
 set Address to "0000000000000"
 set DQ  to "1111111111111111"
 set CK  to "1"
 set CK_ to "0"
 set CKE      to "0"
 set COMMAND  to "1zzz"
 !!set DM   to "00"
 set BA0  to "0"
 set BA1  to "0"
 set BA2  to "0"
 set DQS  to "0101"
 set RES  to "0"
end vector

vector Keep_Control
 drive DQ, DQS
 set Address to "kkkkkkkkkkkkk"
 set DQ to "kkkkkkkkkkkkkkkk"
 set CK       to "k"
 set CK_      to "k"
 set CKE      to "k"
 set COMMAND  to "kkkk"
 !!set DM   to "kk"
 set BA0  to "k"
 set BA1  to "k"
 set BA2  to "k"
 set DQS  to "kkkk"
 set RES  to "k"
end vector
```

8. Once the DDR3 library has been modified, regenerate the silicon nail test.

	Chain Name	Test Name	Test Type	Status
1	U912_U52	sn_U901	Silicon Nail	Generated

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